

# FARHAD EBRAHIMI

Lecturer | Research Assistant

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## EXPERIENCE

Lecturer | M.Sc & B.Sc Thesis supervisor

FAU Erlangen-Nürnberg Technische Fakultät

📅 Oct 2022 – Ongoing  Erlangen, Bavaria

- Lecture: Architecture of supercomputers
- Supervised Master Thesis: FPGA Implementation of a Real-Time Application Based on RISC-V Cores (in cooperation with Siemens)
- Wallace Tree Multiplier, SRT Division integration to RISC-V on FPGA

Research Assistant

FAU Erlangen-Nürnberg Technische Fakultät

📅 April 2022 – Ongoing  Erlangen, Bavaria

- **NOVA**: Non-volatile ternary processors based on the free processor instruction set architecture RISC-V".

## SELECTED PROJECTS

- Design and Implementation of a 7-stage Ternary RISC-V processor supporting RV32Izmmul\_zicsr ISA extension on an FPGA (RTL Design - Zynq™ 7000 & Zynq™ UltraScale+)
- Integration of custom instructions into the RISC-V Architecture & GNU-RISC-V-Toolchain supporting CSD arithmetic calculation
- Design of a Simple System-on-Chip (SoC) using Vivado & Modelsim simulators, featuring a CPU, Histogram, and MAC IPs, all interconnected via the Wishbone Bus (RTL).
- Initiated Petalinux with an Ubuntu rootfs for development on the Ultra-scale+ family and developed drivers to interface with the PL IP core.
- Systolic Array for Matrix Multiplication Acceleration on FPGA (RTL).

## PUBLICATIONS

 **Journal | Conference**

- A. Abdelhafez, F. Ebrahimi Azandaryani, M. Bianconi, and D. Fey, "FPGA Implementation of a Real-Time Application Based on RISC-V Cores," *IEEE International Multi-Conference on Systems, Signals and Devices (SSD)*, 2025.
- F. Ebrahimi Azandaryani and D. Fey, "CSD-Driven Speedup in RISC-V Processors," *Design and Architectures for Signal and Image Processing (DASIP) | HiPEAC*, 2025.
- F. Ebrahimi Azandaryani and D. Fey, "Extern: Boosting RISC-V Core Performance using Ternary Encoding," *Microprocessors and Microsystems*, vol. 107, 2024.
- F. Ebrahimi Azandaryani, O. Akbari, M. Kamal, A. A. Kusha, and M. Pedram, "Accuracy configurable adders with negligible delay overhead in exact operating mode," *ACM Transactions on Design Automation of Electronic Systems*, 2022.
- F. Ebrahimi Azandaryani, O. Akbari, M. Kamal, A. Afzali-Kusha, and M. Pedram, "Block-based carry speculative approximate adder for energy-efficient applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, 2019.

## EDUCATION

M.S. in Computer Science

University of Tehran

📅 Sept 2016 – Feb 2019

B.S. in Computer Science



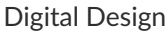

Hamedan University of technology

📅 Sept 2010 – Jan 2015

## SKILLS

VHDL/Verilog  Vivado  Modelsim  
Design Compiler & Prim Time  FPGA  
C/C++/SystemC  openMP & CUDA  
VScode  Version control  Github/lab

## FIELD OF INTEREST

Computer Architecture  CPU & RISC-V  
HW Accelerator  Computer Arithmetic  
Approximate computing  Digital Design  
ASIC/FPGA  Re-configurable computing

## LANGUAGES

German   
English   
Azerbaijani   
Persian/Farsi 

## REFEREES

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