

## Abstract

With CPU microarchitectures becoming increasingly complex, academic lectures about computer architecture and organization have a need for easily graspable teaching methods in order to convey this knowledge to students. To help doing this, a RISC-V pipelining simulator called VAPOR (Visualizer for Advanced Pipelining on RARS) was developed with the goal of improving understanding of CPU pipelining and optimization of assembly programs when compared to typical written tasks. The effectiveness was analyzed in a university course through A/B testing during in-person exercise sessions, splitting them into two possible groups. These sessions differed to either have their first task done on paper or with VAPOR, changing the way how pipelining is introduced during the sessions. For the following tasks, both groups used the simulator. Through a telemetry system, the engagement and performance metrics of 139 participating undergraduate students were gathered during exercise sessions and homework assignments. Analysis of in-person exercises and homework revealed that students utilizing the simulator completed initial tasks more quickly during exercise sessions, with the median student performance being 18% better. However, no measurable impact on performance was observed between the two groups during tasks once both groups used VAPOR. This suggests that student performance is not influenced by the way in which the topic of pipelining is first introduced.